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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,568	01/13/2004	Seiki Ogura	HALO99-006BB	3526

7590 01/10/2006

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,568	OGURA ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *81-83 and 87-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *81-83 and 87-95* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 11/30/2005 has been entered.

2. Claims 81-83,87-95 are presented for examination.

Response to Arguments

3. Applicant's arguments filed 11/30/2005 have been fully considered but they are not persuasive. The double patenting rejection of claims in presented application with claims in application number 09/839,966 now is U.S. Patent No. 6,696,632.

Claims 81, 87-98 are the same invention in claims 12-15 of U.S. Patent No. 6,696,632.

Claim 82 is the same invention in claims 4 and 8 of U.S. Patent No. 6,696,639.

Claims 82 and 93 are the same invention in claims 4 and 8 and 9 of U.S. Patent No. 6,696,639.

Claims 82 and 90 are the same invention in claim 16 of U.S. Patent No. 6,696,639.

Claims 82 and 90 and 91 are the same invention in claims 16 and 17 of U.S. Patent No. 6,696,639.

Claims 82 and 90 and 92 are the same invention in claims 16 and 18 of U.S. Patent No. 6,696,639.

4. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Title

6. The title of the invention in amendment filed on 11/30/2005 is not same original application.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 83, 94-95 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 83, 94-95 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the reply filed 11/30/2005. In that paper, applicant has stated second voltage opposite to first voltage, and this statement indicates that the invention is different from what is defined in the claim(s) because examiner can not find in specification of presented application that a method of erasing a block of nitride regions providing a first voltage and a second voltage, which opposite first voltage in absolutely value as defined in claims 83.

Applicant is required to show it.

Double Patenting

9. Claims 81,87-89, 82,90-93 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 12-15, 4,8-9, 16-18 of prior U.S. Patent No. 6,686,632. This is a double patenting rejection.

Regarding claim 81, 87-89, Ogura et al. (U.S. Patent No. 6,686,632) disclose a method of reading a MONOS memory cell, wherein the MONOS memory cell comprises: a word gate on the surface of a semiconductor substrate; sidewall control gates on sidewalls of said word gate, separated from said word gates by an insulating layer; nitride regions within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions; a polysilicon word line overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates; wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein a read operation of said cell is performed by: over-riding said unselected nitride region; providing a voltage on said word gate having a sum of the word gate threshold voltage, an overdrive voltage, and the voltage on said source diffusion; providing a voltage on said control gate adjacent to said selected nitride region sufficient to allow for reading of the selected nitride region; and reading said cell by measuring the voltage level on said

bit diffusion, and wherein said memory cell is one of many cells in a MONOS memory array, and further comprising applying a control gate voltage of 0 volts to all cells beside the cell desired to be read, and wherein said memory cell is one of many cells in a MONOS memory array, and further comprising applying a control gate voltage of -0.7 volts to all cells beside the cell desired to be read in order to stop leakage, and wherein a voltage level on said bit diffusions represents one of multiple threshold levels of said cell (Claims 12-15).

Regarding claims 82, 90-93, Ogura et al. (U.S. Patent No. 6,686,632) disclose a method of programming a MONOS memory cell, wherein said MONOS memory cell comprises: a word gate on the surface of a semiconductor substrate; sidewall control gates on sidewalls of said word gate, separated from said word gates by an insulating layer; nitride regions within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions; a polysilicon word line overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates; wherein one of said control gates is a selected control gate and its underlying nitride region is a selected nitride region, and the other of said control gates is an unselected control gate and its underlying nitride region is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein said method of programming the cell comprises the steps of:

providing a high voltage on said unselected control gate to over-ride said unselected nitride region', and varying a voltage on said selected control gate, and further comprising: raising a control gate voltage of said selected nitride region; providing a fixed voltage on said bit diffusion; providing a voltage on said word gate which is greater than said word gate threshold voltage; and lowering a voltage of said source diffusion such that current flows from said source diffusion to said bit diffusion wherein ballistic injection of electrons occurs from a channel region to said selected nitride region when current flows and wherein multiple thresholds can be programmed by varying a voltage on said bit line diffusions, and wherein said memory cell is one of many cells in a MONOS memory array, and further comprising disabling nitride regions in adjacent cells sharing a word line by applying a control gate voltage of 0 volts to said adjacent cells, and wherein said memory cell is one of many cells in a flash memory array that share a word line, and further comprising simultaneously programming several of said cells with different threshold levels by varying a voltage either of said sidewall control gates or said bit line diffusions (Claims 4,6,9, 16-19).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827